REMARKS

This response responds to the Office Action dated November 6, 2002 in which the Examiner rejected claims 7-8 under 35 U.S.C. §103.

Claim 7 claims a connection structure comprising a substrate and surface-mounted component. The substrate has a surface and substrate-side pad electrodes formed on the substrate surface. The surface-mounted component has a surface, component-side pad electrodes formed on the surface and a solder bump formed on the component-side pad. The surface is opposed to the substrate with each component-side pad electrode opposed to one of the substrate-side pad electrodes. The substrate-side electrodes are arranged inside a component-corresponding region. The length of each of the substrate-side pad electrodes is larger than that of the corresponding component side pad electrodes. Each of the component-side pad electrodes is connected to the corresponding substrate-side pad electrodes by a solder which has flowed between the component-side pad electrodes and the substrate-side pad electrode by melting of the solder bump. The solder bump is arranged so that a center of the solder bump is located off-set from a center of the substrate-side pad.

Through the structure of claimed invention having a solder bump on a component-side pad arranged so that a center of the solder bump is located off-set from a center of a substrate-side pad, as claimed in claim 7, the claimed invention provides a connection structure in which a pass/fail determination of a connection state is easy to determine. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claims 7 - 8 were rejected under 35 U.S.C. §103 as being unpatentable over *Tanaka* (U.S. Patent No. 5,889,326) in view of *Hiruta* (U.S. Patent No. 5,998,861),

Ohuchi et al. (U.S. Patent No. 6,130,480) and *Eichelberger et al.* (U. S. Patent No. 6,426,545).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to claims and allows the claims to issue.

Tanaka appears to disclose a structure for bonding a semiconductor device to a substrate which is provided with: an A1 pad 2 formed on a semiconductor chip 1; a first bump 4 which is composed of a first metal such as Au and which is formed on the pad 2; a plurality of rectangular substrate pads 6 which are arranged on a circuit board 5 at predetermined pitches, and length L of a first side thereof in parallel to the arranging direction is smaller than length M of a second side thereof which is orthogonal to the first side, length L of the first side is smaller than the diameter of the first bump 4, and length M of the second side is larger than the diameter of the first bump 4; and a second bump 7 which is formed on the substrate pad 6, which melts to cover the first bump 4, and which is composed of a second metal such as eutectic Sn/Pb or other metal that is different from the first metal, the width thereof in the direction parallel to the first side being smaller than the diameter of the first bump 4 and the width thereof in the direction parallel to the second side being larger than the diameter of the first bump 4. (col. 3, lines 7-25).

Thus, *Tanaka* merely discloses in Figs. 2-7 solder bumps centered over substrate pads. Nothing in *Tanaka* shows, teaches or suggests that the solder bump is off-set as

claimed in claim 7. Rather, *Tanaka* teaches away from the claimed invention since the solder bump is centered over the substrate pad.

Hiruta appears to disclose FIG. 1 shows a conventional semiconductor device having a ball grid array. Ball bumps 2 are formed on a main surface of an LSI (large scale integrated circuit) chip 1. The bumps 2 are formed of metal such as solder. A chip carrier 3 comprises a laminate board 4 having a plurality of layers, wires 5 passing through each layer and each interlayer, electrodes 6a formed on one surface side of the laminate board 4, and electrodes 6b formed on the other surface side of the laminate board 4. The wires 5 electrically connect the electrodes 6a to the electrodes 6b. The electrodes 6b are arrayed on the other surface side of the laminate board 4. Ball electrodes 7 are formed on the electrodes 6b, respectively. The ball electrodes 7 constitute a ball grid array. The ball electrodes 7 are formed of metal such as solder, etc. The LSI chip 1 is combined with the electrodes 6a of one side of the laminate board 4 by the ball bumps 2. As a result, the LSI chip 1 is brought into contact with the ball electrodes 7. The following will explain the features of the above-explained semiconductor device having the ball grid array. The first feature lies in that the mount of the semiconductor device can be easily performed. Specifically, as shown in FIG. 2, a semiconductor device 100 is placed on a print circuit board 200, and heat is applied thereon, so that the mount of the semiconductor device can be completed. As shown in FIG. 3, the print circuit board 200 on which the semiconductor device 100 is mounted is moved via a reflow furnace 300. The ball electrodes 7 of the semiconductor device 100 are temporarily melted when entering the reflow furnace 300. Then, when the electrodes 7 come out of the reflow furnace 300, the

ball electrodes 7 are solidified again. At the time when the ball electrodes 7 are solidified again, they are combined with electrodes 8 of the print circuit board 200. (col. 1, lines 10-48)

Thus, *Hiruta* merely discloses that the ball bumps 2 are centered over the electrodes 6a. Nothing in *Hiruta* shows, teaches or suggests that the center of the solder bump is located off-set from a center of a substrate side pad as claimed in claim 7. Rather, *Hiruta* teaches away from the claimed invention since the ball electrode 7 are centered over the electrode 6b.

Eichelberger et al. appears to disclose structures and methods for absorbing stress between a first electrical structure and a second electrical structure connected together, wherein the first and second structures have different coefficients of thermal expansion. (col. 1, lines 24-28) FIG. 1a shows a typical printed circuit board 100, such as a FR4 printed circuit board, with through holes 105 plated with two-sided metallization 110. The through holes 105 are filled 115 to prevent subsequently applied dielectric from flowing out through the holes. (col. 6, lines 4-8) FIG. 1c shows the printed circuit board 100 with the LMHE dielectric 120 with via holes and patterned metallization 130. (col. 7, line 66 through col. 8, line 1) It should be noted that specially configured metallization 130 which for each interconnect conductor 135 is disposed above LMHE dielectric 120, the conductor 135 has a length L that is greater than the maximum relative displacement between the first and second electrical structures due to thermal expansion. (col. 8, lines 9-15) FIG. 1d, a solder mask 140 is patterned on the top surface of the dielectric. Solder paste 145 is stenciled in areas overlying the patterned metallization above the LMHE dielectric. FIG. 1e shows a bumped

150 die 160 soldered to the patterned metallization 130 above the LMHE dielectric. (col. 9, lines 17-21)

Thus, *Eichelberger et al.* merely discloses solder balls 250, 350 formed between metal layer 230, 330 and stenciled solder paste 445. Nothing in *Eichelberger et al.* shows, teaches or suggests a solder bump on a component-side pad arranged so that a center of the solder bump is located offset from a center of a substrate-side pad as claimed in claim 7. *Eichelberger et al.* only discloses solder balls formed between a metal layer and a solder paste.

Furthermore, Applicants respectfully traverse the Examiner's statement that the solder connection in *Eichelberger et al.* is offset. Nothing in *Eichelberger et al.* shows, teaches or suggests this feature or the importance thereof. Applicants further traverse the Examiner's statement that the Applicants have not claimed any specific advantage/disadvantage of keeping center of the solder bump in the center of the substrate pad. Applicants respectfully bring the Examiner's attention to paragraphs [0052] through [0055] of the specification found bridging pages 12 and 13. As explained in these paragraphs, and shown in Figures 3A, 3B, 4A and 4B, when the melted solder 3A has not spread over the entire surface of the substrate-side pad electrode 12 (12a), no x-ray non-transmission portion is observed while on the other hand when the melted solder 3A has spread over the entire surface of the substrate-side pad, it is easy to recognize x-ray non-transmission portion as a whole. In particular, please compare Figure 3A with Figure 4A and Figure 3B with Figure 4B. Nowhere in *Eichelberger et al.* is it shown, taught or suggested to detect the connection state based upon the location of the solder bump as

claimed in claim 7. Rather, *Eichelberger et al.* is merely directed to absorbing stress between electrical structures having different coefficients of thermal expansion.

Ohuchi et al. appears to disclose a method for packaging a semiconductor chip such as an LSI chip or the like on a circuit substrate. (col. 1, lines 6-8) FIG. 1 is a cross-sectional view showing a structure for packaging a semiconductor chip comprises a semiconductor chip 1 having a plurality of bumps 3 formed on a circuit forming surface thereof which serves as a lower surface thereof as seen in the drawing, a substrate 2 on which copper-made wiring patterns 5 with the bumps 3 joined thereto are formed so as to correspond to forming positions of the bumps 3, and a polyimide tape 8 having adhesive layers 9 provided on both surfaces thereof. A spacing defined between the semiconductor chip 1 and the substrate 2 is sealed with a resin layer 7. Through holes 2a, which extend through the substrate 2, are defined in the substrate 2 at their corresponding positions where the wiring patterns 5 are provided. Solder balls 4 are formed on the back side corresponding to the lower side of the substrate 2 as seen in the drawing as electrodes so that they be electrically connected to their corresponding wiring patterns 5 via the through holes 2a. An insulating film or layer 6 for covering the wiring patterns 5 unjoined to the bumps 3 is formed on the surface of the substrate 2, which is located on the joining side of the semiconductor chip 1. A material for the substrate 2 is selected so that a thermal expansion coefficient of the substrate 2 is substantially equal to that of the polyimide tape 8. (col. 2, line 48 through col. 3, line 7) According to this structure and method, since the semiconductor chip 1 and the substrate 2 are firmly joined to one another by three bonding or joining forces or powers: a joining power developed between the bumps 3 and the wiring patterns 5, a joining power produced by the

polyimide tape 8 and a joining power produced by the sealing resin layer 7, a strong bonding power is obtained even if a joining area of the polyimide tape 8 is small, thereby making it possible to reduce the chance that a contact failure may occur due to deterioration over time. (col. 3, lines 53-63)

Thus, *Ohuchi et al.* merely discloses in Figure 1 bumps 3 formed on a semiconductor chip 1 and serving as a lower surface of the chip connected to wiring patterns 5. Nothing in *Ohuchi et al.* shows, teaches or suggests a solder bump on a component-side pad arranged offset from a center of substrate-side pad as claimed in claim 7. Rather, the plurality of bumps 3 of *Ohuchi et al.* are not formed of solder (see solder balls 4), and are not arranged on a component-side pad. The bumps 3 of *Ohuchi et al.* are only formed on a lower surface of a semiconductor chip and are arranged to connect to wiring patterns 5 and not to a substrate-side pad.

Applicants again respectfully traverse the Examiner's statement that Applicants have not claimed specific advantage/disadvantage of centering the solder bump on the substrate pad. Again, Applicants respectfully bring the Examiner's attention to pages 12 and 13 and Figures 3A, 3B, 4A and 4B of the specification. Furthermore, Applicants respectfully point out that *Ohuchi et al.* is directed to a method of packaging a semiconductor chip and is not directed to a connection structure in which the connection state is easy to determine.

Since nothing in *Tanaka, Hiruta, Eichelberger et al.* or *Ohuchi et al.* show, teach or suggest a solder bump on a component-side pad arranged so that a center of the solder bump is located offset from a center of a substrate-side pad as claimed in claim 7, it is

respectfully requested that the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §103.

Claim 8 depends from claim and recites additional features. It is respectfully submitted that claim 8 would not have been obvious within the meaning of 35 U.S.C. §103 over *Tanaka, Hiruta, Eichelberger et al.* and *Ohuchi et al.* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 8 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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